XR5352

18V/2A

Sync. Step-Down Converter

DESCRIPTION

The XR5352 are monolithic buck switching regulators based on I2 architecture for fast transient response. Operating with an input range of 4.5V~18V, XR5352 deliver 2A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, XR5352 operates in low frequency to maintain high efficiency.

XR5352 guarantees robustness with output short protection, thermal protection, current run-away protection and input under voltage lockout.

XR5352 is available in SOT23-6 package, which provides a compact solution with minimal external components.

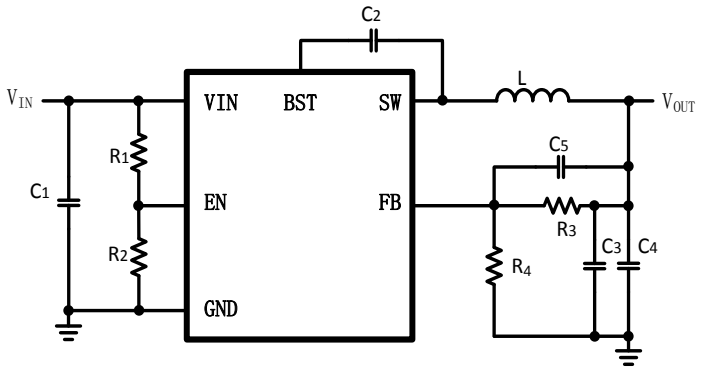
FEATURES

- 4.5V to 18V operating input range
  2A output current
- Up to 95% efficiency
- PFM at light load
- 600kHz switching frequency
- Internal soft-start
- Input under-voltage lockout
- Current run-away protection
- Output short protection
- Thermal protection
- Available in SOT23-6 package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

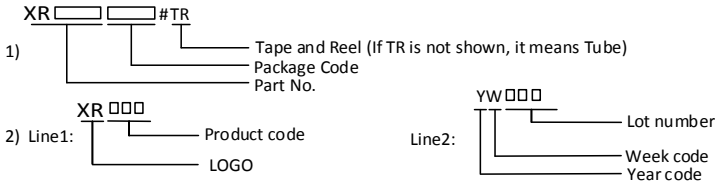
TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
XR5352SOTB#TR	SOT23-6		Green

Notes:



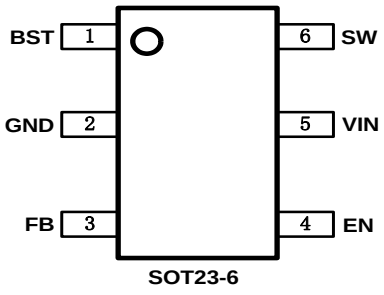
3) All products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

DEVICE INFORMATION

DEVICE	Operation Mode at light load	Function	Package
XR5352SOTB#TR	PFM	-	SOT23-6

PIN CONFIGURATION

TOP VIEW



SOT23-6

ABSOLUTE MAXIMUM RATING[1)]

VIN, EN Pin…… KKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKKK -0.3V to 20V
SW Pin……..……-0.3V(-5V for 10ns) to 20V(22V for 10ns)
BST Pin..... SW-0.3V to SW+4V
All other Pins ..... -0.3V to 4V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature .....-65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS

Input Voltage V_{IN} .....4.5V to 18V
Output Voltage V_{OUT} .....0.6V to V_{IN}*D_{max}

THERMAL PERFORMANCE

	θ_{JA}	θ_{Jc}
SOT23-6[3)]	220	130ºC/W
SOT23-6[4)]	140	75ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The XR5352 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) Measured on JESD51-7, 4-layer PCB.

4) Measured on a two-layer XR5352 Evaluation Board at T_A=25℃.

ELECTRICAL CHARACTERISTICS

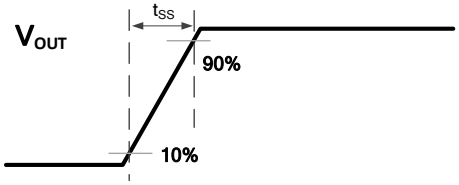
VIN=12V, T_A=25℃, Unless otherwise stated。

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lockout Threshold	V_{IN_MIN}	V_{IN} rising		4.2		V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			300		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		0.1		μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1V		100		μA
Feedback Voltage	V_{FB}	4.5V<V_{VIN}<18V		600		mV
Top Switch Resistance	$R_{DS(ON)T}$			130		mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$			70		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=18V, V_{EN}=0V, V_{SW}=0V		0.1		μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=18, V_{EN}=0V, V_{SW}=18V		0.1		μA
Bottom Switch Current Limit	I_{LIM_BOT}			2.7		A
Minimum On Time[5)]	T_{ON_MIN}			120		ns
Minimum Off Time	T_{OFF_MIN}	V_{FB}=0.4V		150		ns
Maximum On Time	T_{ON_Max}			4		us
EN Rising Threshold	V_{EN_H}	V_{EN} rising		1.2		V
EN Falling Threshold	V_{EN_L}	V_{EN} falling		1.05		V
Soft-Start Period[5)6)]	t_{SS}			1.4		ms
Frequency	f_{SW}			600		kHz
Thermal Shutdown[5)]	T_{TSD}			160		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			20		°C

Note：

5) Guaranteed by design.

6) Soft-Start Period is tested from 10% to 90% of the steady state output voltage.

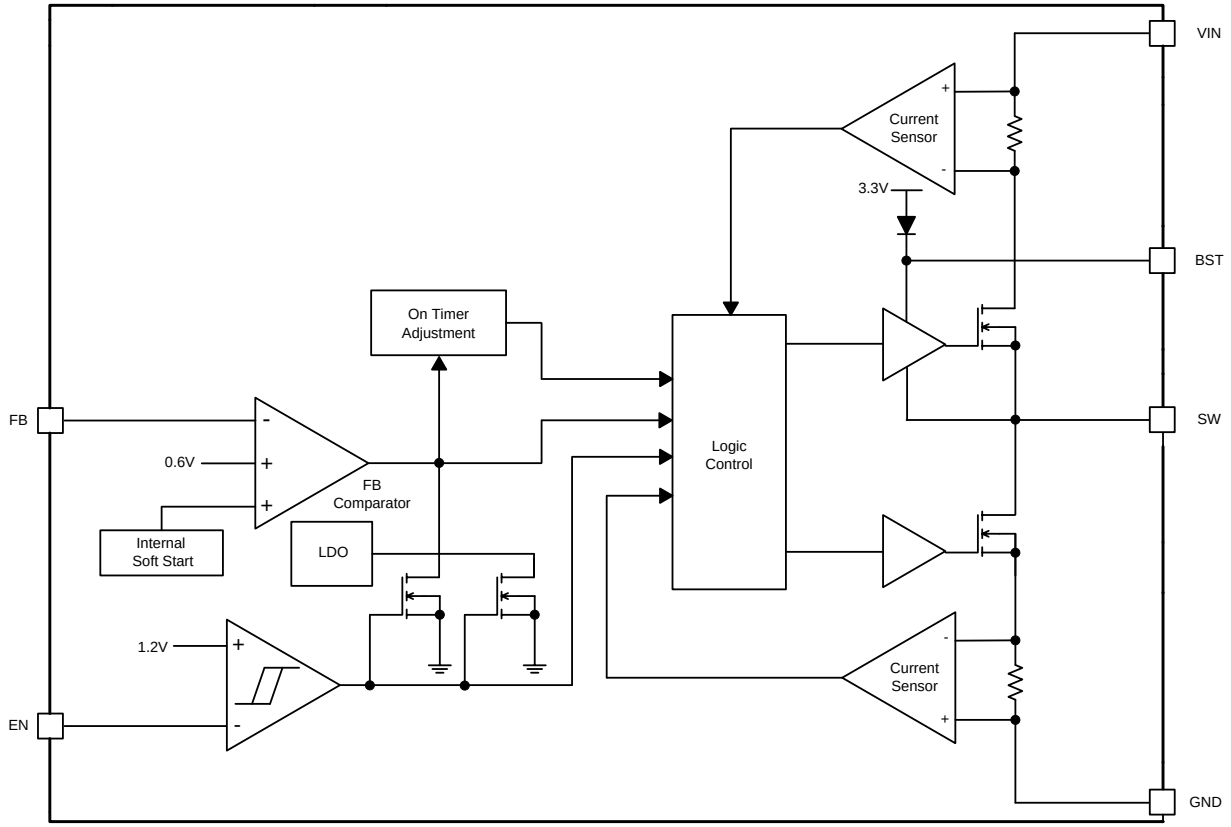


t_{SS} Waveform

PIN DESCRIPTION

SOT23-6	Name	Description
1	BST	Connect a 0.1μF capacitor between BST and SW pin to supply voltage for the top switch driver.
2	GND	Ground pin.
3	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
4	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
5	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

XR5352 is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 4.5V to 18V down to an output voltage as low as 0.6V, and is capable of supplying up to 2A of load current.

Shut-Down Mode

The regulator shuts down when voltage at EN pin is driven below 0.4V. The entire regulator is off and the supply current consumed by the regulator drops below 1μA.

Power Switch

N-Channel MOSFET switches are integrated on the XR5352 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.3V rail when SW is low.

V_{IN} Under-Voltage Protection

A resistive divider can be connected between V_{IN} and ground, with the central tap connected to EN, so that when V_{IN} drops to the pre-set value, EN drops below 1.05V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current. A valley current limit is designed in XR5352 so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 2048 cycles. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 2048 switching cycles, then no switching is allowed and the regulator enters hiccup mode for 6144 cycles. After the 6144 hiccup cycles, the regulator will try to start-up again. If the short condition still exists after 2048 cycles of switching, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

Thermal Protection

When the temperature of the regulator rises above 160°C, it is forced into thermal shut-down. Only when core temperature drops below 140°C can the regulator become active again.

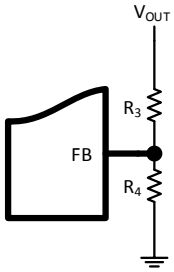
APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_4}{R_4 + R_3}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintain the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

The input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimize the potential noise, a small X5R or X7R ceramic capacitor, e.g. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22μF/25V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, and lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 22μF~66μF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output

voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1μF low ESR ceramic capacitor is recommended to be connected between the BST pin and SW pin.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to follow the guidelines as below.

1. Place the input decoupling capacitor as close to XR5352 (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as

SOT23-6:

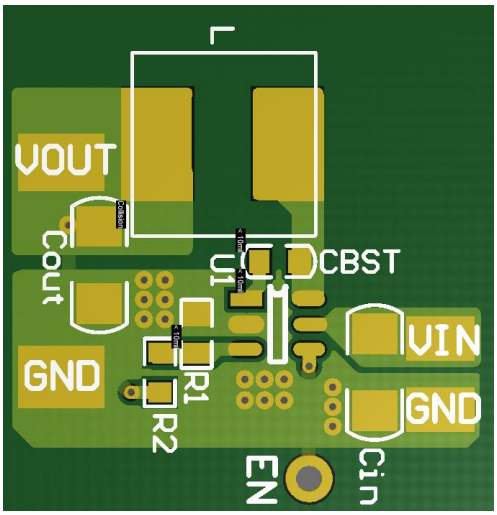
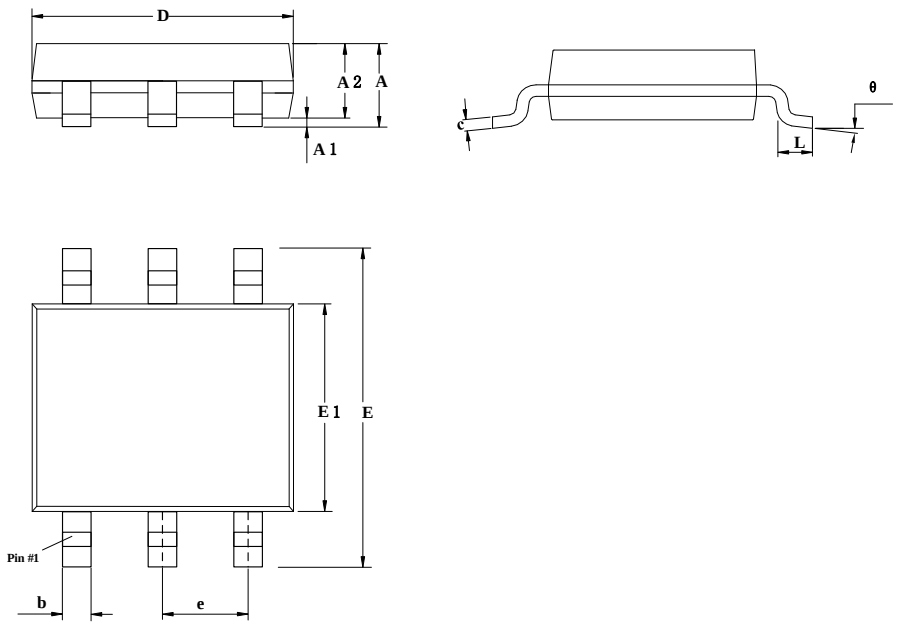


Figure1. PCB Layout Recommendation

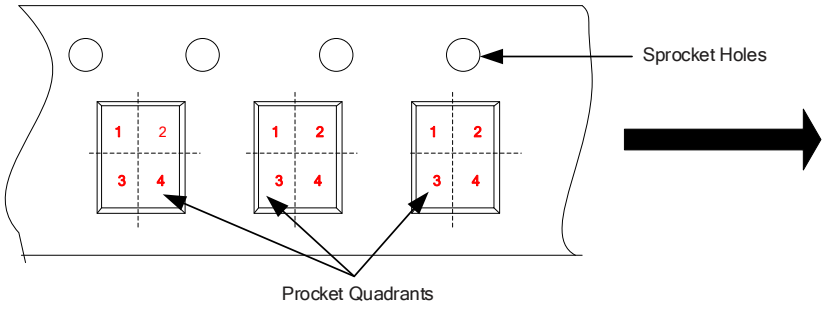
PACKAGE OUTLINE

SOT23-6 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.15	1.25
A1	0	0.05	0.15
A2	0.95	1.10	1.20
b	0.30	0.40	0.50
c	0.05	—	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95（BSC）		
L	0.30	0.45	0.60
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package Type	Pin1 Quadrant
SOT23-6	3