Application Note: AN_SY7200A

30V High Current Boost LED Driver
Preliminary Specification

General Description

SY7200A is DC/DC step-up converter that deliver an accurate constant current for driving LEDs. Operation at a fixed switching frequency of 1MHz allows the device to be used with small value external ceramic capacitors and inductor. LEDs connected in series are driven with a regulated current set by the external resistor. The SY7200A is ideal for driving up to eight white LEDs in series or up to 30V.

Ordering Information

SY7200 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Dimming
SY7200AABC	SOT23-6	20kHz~1MHz

Features

- Input voltage range: 2.8 to 30V
- Switch current limit 2A
- Drives LED strings up to 30V
- 1MHz fixed frequency minimizes the external components
- Dimming frequency for EN/PWM pin: 20kHz~1MHz
- Internal softstart limits the inrush current
- Open LED over voltage protection
- RoHS Compliant and Halogen Free

Applications

- GPS Navigation Systems
- Handheld Devices
- Portable Media Players

Typical Applications

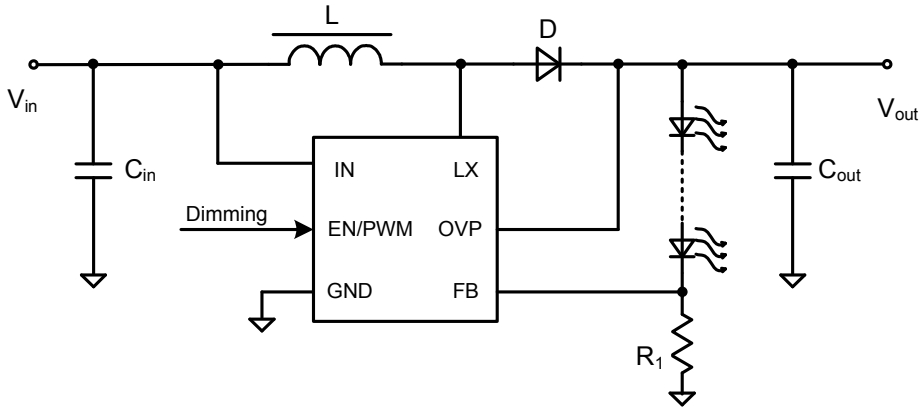
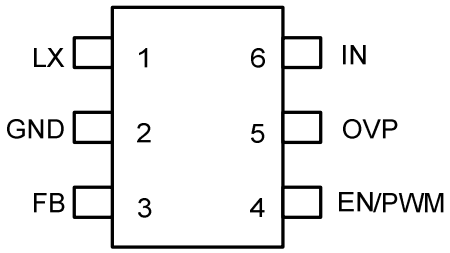


Figure 1. Schematic Diagram

Pinout (top view)



(SOT23-6)

Top mark: **HY*xyz*** (Device code: HY, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
LX	1	Inductor node. Connect an inductor between IN pin and LX pin.
GND	2	Ground pin.
FB	3	Feedback pin. Connect a resistor R1 between FB and GND to program the output current: I_{OUT}=0.2V/R_1.
EN/PWM	4	Enable and dimming control. When used as enable input, pull high to turn on IC. When used as dimming input, the first pulse should be longer than 200ns to turn on IC. And the recommend dimming frequency range is 20kHz~1MHz.
OVP	5	Over voltage protection. The typical value is 30V.
IN	6	Input pin. Decouple this pin to GND pin with ceramic capacitor.

Absolute Maximum Ratings (Note 1)

IN, EN ---------- 32V
LX, OVP ---------- 36V
All other pins ---------- 4V
Power Dissipation, P_D @ T_A = 25°C, SOT23-6 ----------0.6/0.55W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 170/180°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Input Voltage Supply---------- 2.8V to 30V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.8		30	V
Quiescent Current	I_Q	V_{FB}=0.3V		0.1	0.6	mA
Shutdown Current	I_{SHDN}	EN=0		10	15	uA
Feedback Reference Voltage	V_{REF}		196	200	204	mV
FB Input Current	I_{FB}	V_{FB}=0.3V			1	uA
Low Side Main FET RON	$R_{DS(ON)}$			220		mΩ
Main FET Current Limit	I_{LIM}		2			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.7	V
UVLO Hysteresis	V_{HYS}			0.1		V
Oscillator Frequency	F_{OSC}	I_{OUT}=100mA		1.0		MHz
Min On Time				100		ns
Max Duty Cycle				90		%
Thermal Shutdown	T_{SD}			150		℃
Thermal Hysteresis	T_{HYST}			20		℃
Output Clamp voltage	V_{OCL}	“Open LED”		30		V
PWM dimming frequency			20k		1M	Hz

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

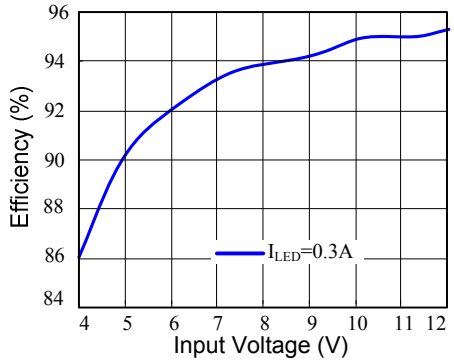
Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

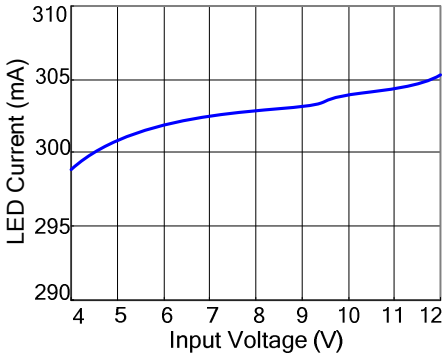
Typical Performance Characteristics

(V_{IN}=5V, I_{LED}=0.3A, 5PCS LED Series)

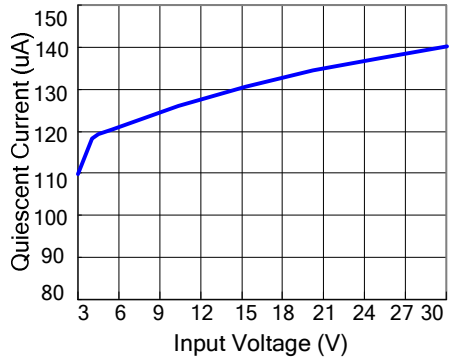
Efficiency vs. Input Voltage



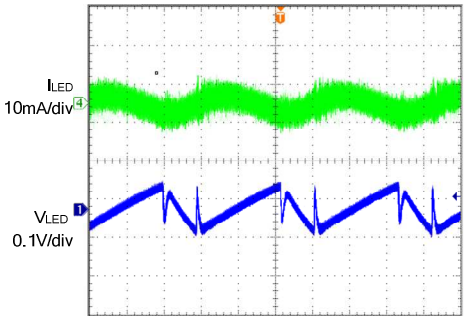
LED Current vs. Input Voltage



Quiescent Current vs. Input Voltage

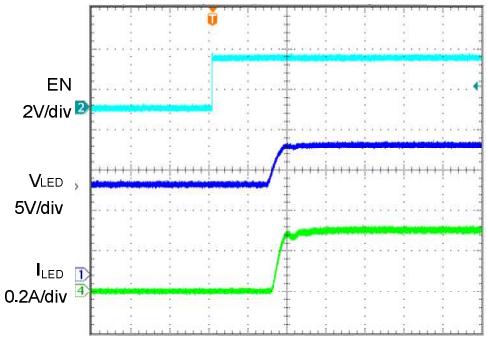


LED Current Pripple



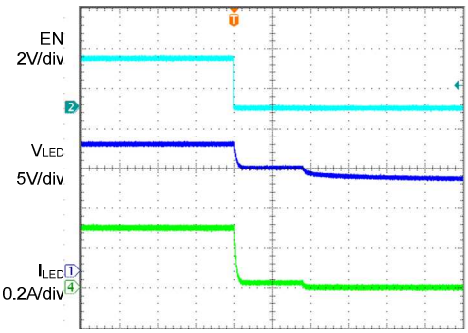
Time (200ns/div)

Startup from Enable



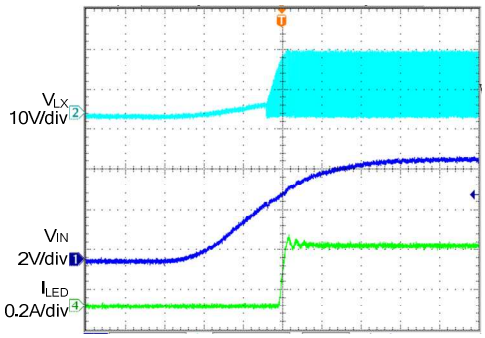
Time (100us/div)

Shutdown from Enable



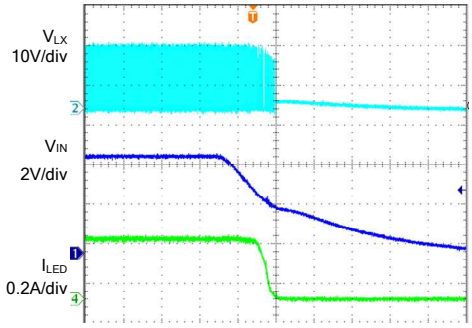
Time (1ms/div)

Starup from V_{IN}



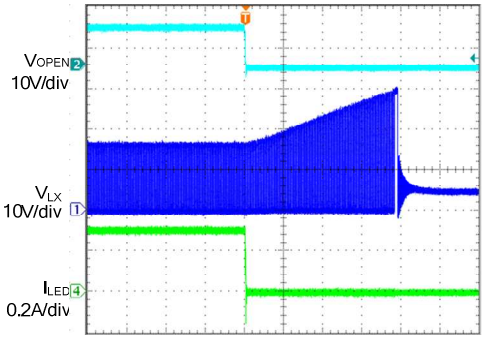
Time (200us/div)

Shutdown from V_{IN}



Time (2ms/div)

"Open LED"Protection



Time (10us/div)

Applications Information

Because of the high integration in the SY7200A IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, Schottky diode D and sense resistors R1 need to be selected for the targeted applications specifications.

Sense resistor R1 :

Choose R1 to program the proper LED Current. The R1 can be calculated to be:

$$R1 = \frac{0.2}{I_{LED}}$$

I_{LED} is the average LED current.

Input capacitor CIN:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

A typical X7R or better grade ceramic capacitor with larger than 4.7uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins.

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X7R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT} = \frac{I_{OUT,\,MAX} \cdot (V_{OUT} - V_{IN})}{F_{SW} \cdot V_{OUT} \cdot V_{RIPPLE}}$$

V_{RIPPLE} is the peak to peak output ripple.

For LED applications, the equivalent resistance of the LED is typically low. The output capacitance should be large enough to attenuate the ripple current through LED. A capacitor larger than 2.2uF is recommended.

Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,\,MAX} \times 40\%}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY7200A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Schottky Diode D:

Because of high switching speed of SY7200A, a Schottky diode with low forward voltage drop and fast switching speed is desirable for the application. The voltage rating of the diode must be higher than maximum output voltage. The diode's average and peak current rating should exceed the average output current and peak inductor current.

Layout Design:

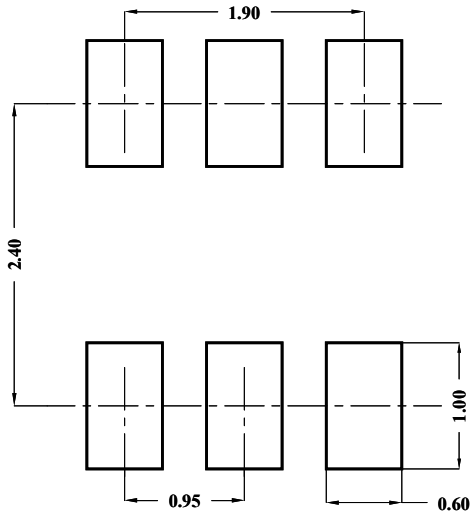
The layout design of SY7200A regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{OUT}, L, R1 and D.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

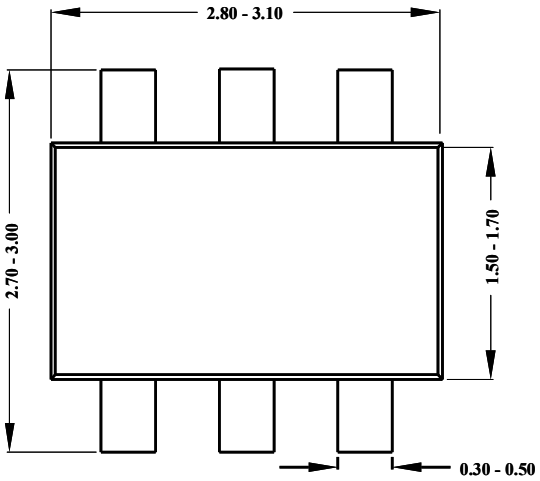
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

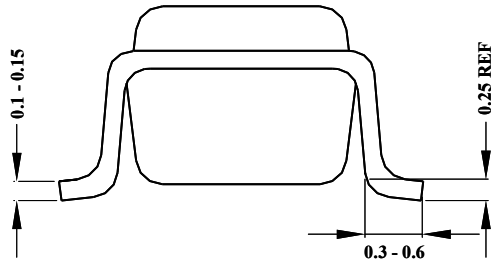
3) Minimize the loop area of LX, D, C_{OUT} and GND.
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
5) The components R1, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

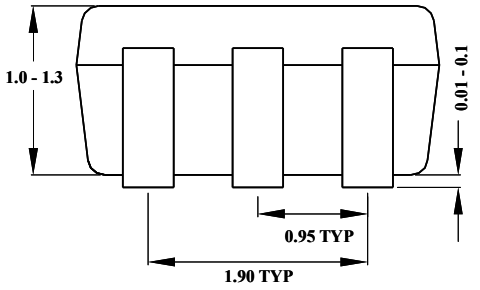
SOT23-6 Package outline & PCB layout design



Recommended Pad Layout





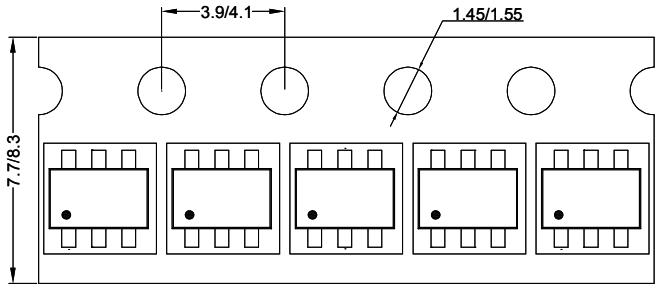


Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

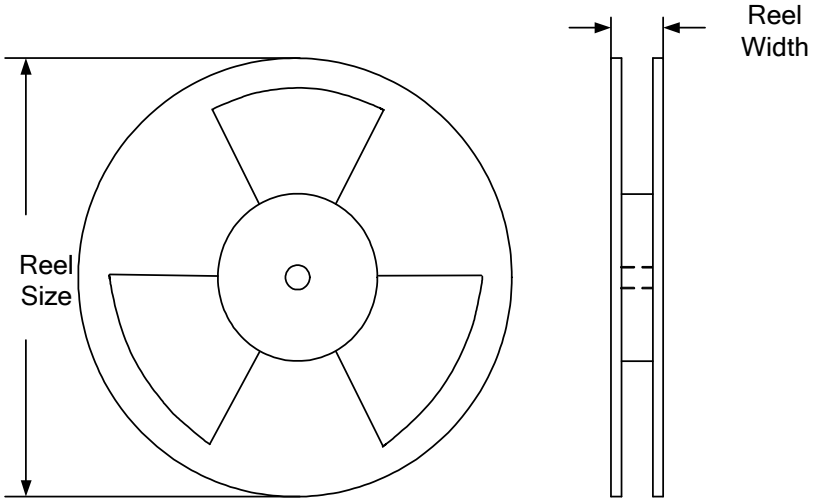
1. Taping orientation

SOT23-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	8.4	280	160	3000

3. Others: NA